APPLICATION NO. 09/956986

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Claim 1 (currently amended): A semiconductor device comprising:

a semiconductor layer;

a first insulating film formed on said semiconductor layer;

a first electrode layer formed on said first insulating film;

element isolating regions comprising of an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating regions isolating an element region and being self-aligned with said first electrode layer;

a second insulating film formed on said first electrode layer across said element isolating regions, said second insulating film having an open portion exposing a surface of said first electrode layer, ~~said open portion being located at a center portion of the second insulating film,~~ and said element isolating ~~insulation~~ insulating film being located under the open portion and having a groove having a shape which is the same as that of the open portion; and

a second electrode layer formed on said second insulating film and said exposed surface of said first electrode layer, said second electrode layer being electrically connected to said first electrode layer via said open portion, said first and second electrode layers including a gate electrode, said open portion having a first width in a direction of a gate length of said gate electrode and a second width in a direction perpendicular to the direction of the gate length, the second width being greater than the first width, the open portion extending in a direction of the second width across the element isolating regions, and said open portion being located at a center portion of the second electrode layer.

CLAIM 2 (CANCELLED)

Claim 3 (previously presented): The semiconductor device according to claim 1, wherein said gate electrode is a gate electrode of a selective transistor included in a NAND type flash memory.

CLAIM 4 (CANCELLED)

Claim 5 (previously presented): The semiconductor device according to claim 1, which is a semiconductor device in a memory cell array region, comprising:

said semiconductor layer;

said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating film;

said element isolating regions comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating regions isolating an element region and being self-aligned with said first electrode layer;

said second insulating film formed on said first electrode layer and said element isolating regions; and

said second electrode layer formed on said second insulating film;

wherein a surface of said element isolating regions of said memory cell array region is arranged below a surface of said first electrode layer.

CLAIM 6 (CANCELLED)

Claim 7 (original): The semiconductor device according to claim 5, wherein said first electrode layer performs a function of a floating gate and said second electrode layer performs a function of a control gate in said memory cell array region.

CLAIMS 8-10 (CANCELLED)

Claim 11 (previously presented): The semiconductor device according to claim 1, further comprising a connecting member arranged above one of said element isolating regions and electrically connected to said second electrode layer.

CLAIMS 12-13 (CANCELLED)

Claim 14 (previously presented): The semiconductor device according to claim 1, further comprising a wiring electrically connected to said second electrode layer via a connecting member, wherein said wiring and said first electrode layer are connected to each other via said second electrode layer extending from said element region onto one of said element isolating regions.

CLAIM15-31 (CANCELLED)

Claim 32 (previously presented): The semiconductor device according to claim 1, wherein an electric resistance of said second electrode layer is lower than that of said first electrode layer, and said second electrode layer comprises a metal layer including a high melting point or a lamination layer film comprising a metal silicide layer including a high melting point and a polysilicon layer.

CLAIM 33 (CANCELLED)

Claim 34 (previously presented): The semiconductor device according to claim 1, wherein said second insulating film comprises a complex insulating film including a silicon nitride film.

CLAIM 35 (CANCELLED)

Claim 36 (previously presented): The semiconductor device according to claim 1, which is a semiconductor device in which said second insulating film remains at an edge portion of said gate electrode.

CLAIMS 37-60 (CANCELLED)

Claims 61-62 (canceled)